UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,898	09/16/2003	Aron T. Lunde	2269-5457US (01-1366.00/U	4518

24247 7590 07/12/2005

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,898	LUNDE ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-11,13-19* is/are rejected.

7)☒ Claim(s) *6-8,12,20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 9, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Pat. 6486005) in view of Fenner et al. (U.S. Pat. 6627917).

Kim discloses a semiconductor device comprising:

a first functional die 31a including at least a first bond pad 32;

at least a second functional die 31b including at least a second bond pad 32, the at least a second functional die formed as a unitary integral wafer segment with the first functional die (fig. 3A); and

an adjacent die interconnection circuit 38 operably coupling the at least the first bond pad of the first functional die with the at least the second bond pad of the at least the second functional die (fig. 3G, column 3, lines 47 et seq.).

Kim does not disclose that the at least a second functional die maintained as a unitary integral wafer segment with the first functional die .

However, Fenner et al. disclose a semiconductor device comprising: a plurality of dice, wherein at least a second functional die formed and maintained as a unitary integral wafer segment with a first functional die (figs. 1-2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made

to modify the device structure of Kim et al. by having at least a second functional die maintained as a unitary integral wafer segment with a first functional die, as taught by Fenner et al., in order to assure in quality and reduce complexity of implementation of a chip size package (column 2, lines 5-8).

- Regarding claim 2, Kim discloses that the adjacent die interconnection circuit includes at least one conductor segment 38 having a first end electrically coupled to the at least the first bond pad and a second end electrically coupled to the at least the second bond pad (fig. 3G).
- Regarding claim 3, Kim discloses that the adjacent die interconnection circuit further includes a conductive bump 40 electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor device with the substrate contact of a high level packaging element (fig. 3G).
- Regarding claim 4, Kim discloses that the first functional die and the second functional die are immediately adjacent (fig. 3G).
- Regarding claim 9, Kim discloses a segment of a semiconductor wafer, comprising: two functional dice 31a and 31b each including at least one bond pad 32, the two functional dice being on a unitary integral wafer segment (fig. 3A); and an adjacent die interconnection circuit 38 for mutually operably coupling each at least one bond pad of the two functional dice to at least one other bond pad 32 of the two functional dice (fig. 3G, column 3, lines 47 et seq.).

- Regarding claim 11, Kim discloses that the adjacent die interconnection circuit includes at least one conductor segment 38 for coupling between each of the two functional dice, the conductor segment including a first end electrically coupled to the at least one bond pad on one of the two functional dice and a second end electrically coupled to the at least one bond pad on another of the two functional dice (fig. 3G).
- Regarding claim 13, Kim discloses that the two functional dice are immediately adjacent on the segment of semiconductor wafer (fig. 3G).

3. Claims 5, 10, 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Pat. 6,486,005) in view of Fenner et al. (U.S. Pat. 6627917) and further in view of Farnworth et al. (U.S. Pat. 6,744,067).

- Regarding claims 5, 10, 14-15, Kim and Fenner et al. substantially disclose all the limitations as

claimed above except for the first functional die and the second functional die are separated by at least one nonfunctional die.

However, Farnworth et al. disclose that a first functional die and a second functional die are separated by at least one nonfunctional die (column 3, lines 28-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to test the device structure of the above combination by having the nonfunctional die between the first and second functional dice, as taught by Farnworth et al., for testing of each individual die or groups of dice in order to determine and segregate operational dice from nonfunctional die (column 8, lines 25-28).

- Regarding claim 16, Kim discloses that the first functional die and the second functional die are immediately adjacent on the semiconductor wafer (fig. 3G).
- Regarding claim 17, Farnworth et al. discloses that the first functional die and the second functional die are separated by at least one nonfunctional die on the semiconductor wafer (column 3, lines 28-31).
- Regarding claim 18, Kim discloses that the adjacent die interconnection circuit includes at least one conductor segment 38 having a first end electrically coupled to the first bond pad and a second end electrically coupled to the second bond pad for electrically coupling the first bond pad with the second bond pad (fig. 3G).
- Regarding claim 19, Kim discloses that the adjacent ide interconnection circuit further includes a conductive bump 40 electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor wafer with a contact of a higher level packaging (fig. 3G).

Allowable Subject Matter

Claims 6-8, 12 and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose the combination of all the limitations recited, including at least one nonfunctional die including at least one bond pad, the at least one nonfunctional die being formed on the common semiconductor substrate and

located thereon between the first functional die and the at least a second functional die; and wherein the at least one conductor segment extends between the at least a first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the at least a second bond pad (claim 6); at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on the unitary semiconductor wafer segment and located thereon with the two or more functional dice; and wherein the adjacent die interconnection circuit extends between the at least one bond pad of the at least one nonfunctional die to the at least one bond pad of the two or more functional dice (claim 12); and at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on a common semiconductor substrate and located thereon between the first functional die and the second functional die; and wherein the at least one conductor segment extends between the first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the second bond pad (claim 20).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

HOAI PHAM
PRIMARY EXAMINER